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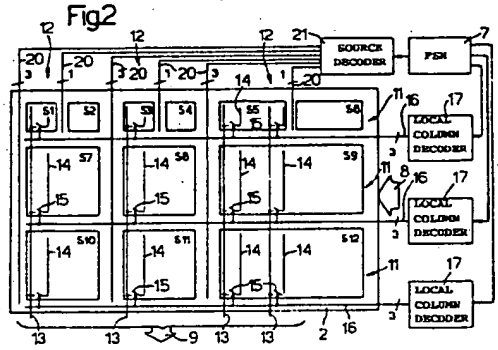
(54) Nonvolatile, in particular flash-EEPROM, memory device

(57) A memory (1) comprising a memory array (2), a row decoding unit (3), a column decoding unit (4), and a control unit (7); the memory array presents global bit lines (13) extending along the whole of the array (2) and connected to respective local bit lines (14), one for each of the sectors; a switch (15) is provided between the global bit lines (13) and each respective local bit line (14) to selectively connect a selected global bit line (13) and only one of the associated local bit lines (14); and the switches are controlled by local decoding units (17) over control lines (16), to address the sectors (S1-S12) independently and so perform operations (read, erase, write) simultaneously in two different sectors in different rows and columns.

Fig2



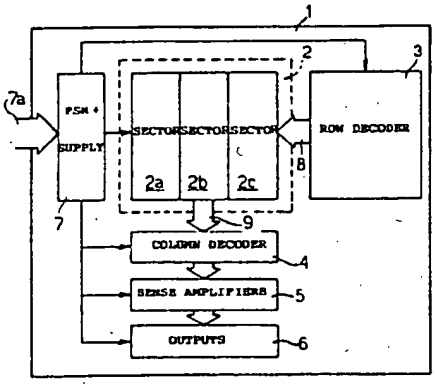


Fig.1

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Description

The present invention relates to a nonvolatile, in particular flash-EEPROM, memory device.

At present, nonvolatile, and in particular flash-EEPROM, memories fail to provide for simultaneously reading one sector and writing or erasing another, which means the memory is blocked and cannot be used for performing other (e.g. read) operations in other sectors until the write or erase operation is terminated. In view of the long time required for erasure, such a limitation is disadvantageous, especially if the memory forms part of a microcontroller, in which case, the microcontroller must comprise appropriate circuits for blocking access to the flash memory, thus increasing the complexity of the system.

For a better idea of the problem underlying the present invention, Figure 1 shows the architecture of a flash memory with sectors organized in columns.

Memory 1 in Figure 1, which only shows the parts pertinent to the present invention, comprises a memory array 2 composed of memory cells organized in rows and columns and addressed by word lines and bit lines shown schematically by arrows 8 and 9; a row decoder 3 from which extend the word lines for biasing the selected row of array 2; a column decoder 4 to which bit lines 9 are connected, and which provides for biasing and connecting the addressed bit line (or lines) of array 2 to the output; a sense amplifying unit 5 in turn comprising a number of sense amplifiers and connected to column decoder 4 to sense the information coded in the memory cells selected by means of decoders 3 and 4; an output unit 6 connected to sense amplifying unit 5, for temporarily retaining the data sensed by unit 5; and a control unit 7 defining, for example, a finite state machine FSM for generating the addresses for row and column decoders 3 and 4, and the control signals for units 5 and 6. For the sake of simplicity, control unit 7 is also assumed to comprise a supply generating section for generating the necessary supply voltages, and to generate the coded addresses supplied from outside memory 1 (arrow 7a) or inside unit 7 according to the operation to be performed (e.g. sequential check of the content of the memory cells during erase).

The cells of array 2 are grouped into sectors; and the cells in the same sector present a common terminal, e.g. the source terminal, so that they are all erased together. In the example shown, the memory cells are grouped into three sectors 2a, 2b, 2c organized in columns, but the following description also applies equally to sectors organized in rows.

To erase a sector, a series of operations is commenced to perform a preconditioning step, and an erase step comprising the actual erase procedure and a verify procedure.

The preconditioning step provides for bringing all the cells in the sector to the same condition prior to actual erasure, and so ensuring they are all erased similarly. For this purpose, the bytes composing the digital words memorized in the cells are addressed successively, and the cells relative to the bytes are written and then verifed using row and column decoders 3, 4 and sense amplifying unit 5. The actual erase and verify procedures also require the use of row and column decoders 3, 4 and unit 5, so that erasure of a sector takes some time (in the order of 1 sec) during which the decoders and amplifying unit 3-5 are engaged in biasing and verifying, and cannot be used for other functions - a situation which is of course undesirable.

It is an object of the present invention to provide a nonvolatile memory device capable of performing different operations in different sectors, e.g. erase one sector while simultaneously reading another.

According to the present invention, there is provided a nonvolatile memory device as claimed in Claim 1.

A number of preferred, non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows the architecture typical of a known memory and also valid for certain embodiments of the present invention;
Figure 2 shows, schematically, the structure of the memory array according to a first embodiment of the present invention;
Figure 3 shows a more detailed view of a variation of the Figure 2 memory array;
Figure 4 shows a logic diagram illustrating the various ways of addressing the Figure 2 and 3 memory;
Figure 5 shows a simplified circuit diagram of one implementation of the row decoder of the memory according to the present invention;
Figure 6 shows a simplified circuit diagram of one implementation of the column decoder of the memory according to the present invention;
Figure 7 shows a further architecture of the memory according to the present invention;
Figure 8 shows a variation of the memory according to the present invention;
Figure 9 shows a further variation of the memory according to the present invention;
Figures 9a and 9b show logic map diagrams relative to a known memory, and relative to the Figure 9 variation of the memory according to the present invention;
Figure 10 shows a further variation of the present invention.

According to a first aspect of the invention, the memory device presents the overall architecture in Figure 1, and the memory array is so formed as to permit a number of operations to be performed simultaneously in different sectors. Figure 2 shows an example embodiment of the memory array, wherein the array 2 comprises twelve sectors S1-S12 of different sizes; sectors S1-S6 being smaller and used for data storage; and

sectors S7-S12 being larger and used for program storage.

Sectors S1-S12 are arranged in rows 11 and columns 12 defining two perpendicular alignment directions. More specifically, sectors S1-S6 are arranged in a first row, sectors S7-S9 in a second row, and sectors S10-S12 in a third row; and, in view of the difference in size, each column comprises two of the smaller sectors, i.e. the first column comprises sectors S1, S2, S7, S10, and so on. For the purpose of the present invention, therefore, i.e. as regards simultaneous addressing of two sectors for read and erase or, at any rate, for performing different operations, each pair of smaller sectors S1-S6 in the same column will hereinafter be considered a single sector. At the expense of a slight increase in complexity and size, however, sectors S1-S6 may also be managed independently.

Global bias lines (in the example shown, global bit lines) 13 extend along the whole of matrix 2 in one of the two alignment directions (in the example shown, along the full length of sector columns 12), and are connected to local bias lines 14 (one for each sector in said alignment direction, and in this case, one for each of the three sectors in the sector column 12 along which the global bit line 13 extends). Between global bias lines 13 and each respective local bias line 14, a switch 15 is provided for selectively connecting a selected global bit line 13 and only one of the three associated local bit lines 14, and so biasing the sectors independently to perform operations (read, erase, write) simultaneously in two different sectors forming part of different lines (rows and columns).

The switches 15 in the same sector are controlled in common (with the exception of sector pairs S1-S2, S3-S4, S5-S6, the sectors in each pair of which are controlled by the same control signal as indicated above) but independently of the other sectors. For this purpose, the control terminals of switches 15 are connected to control lines 16 - one for each sector - connected to one or more local decoders 17. In the Figure 2 example, the control lines 16 relative to sectors in the same row are connected to a respective local column decoder 17.

Figure 2 also shows, schematically, source lines 20 - one for each sector - connected to a source decoder 21 in turn controlled by control unit 7 to bias lines 20 according to the read, write and erase steps of each sector.

To permit operations to be performed simultaneously in sectors S1-S12, appropriate changes must obviously also be made to units 3-5 which may for example be simply duplicated.

A further embodiment of the Figure 2 memory array is shown in Figure 3, which shows a number of the memory cells and the switches of sectors S7-S12 only. The structure shown for sectors S7-S12, however, is also the same for sectors S1-S6.

In the Figure 3 example, each global bit line in each sector is connected to two local bit lines 25 and 26 for better compacting the cells, bearing in mind that the global bit line 13 - typically formed in the second metal level - must be wider than the local bit lines 14 - typically formed in the first metal level - to ensure a sufficient size of the contacts. As such, six control lines 16 are provided for each sector row 11. In Figure 3, provision is also made for only one local column decoder 17' which combines the functions of the three decoders 17 in Figure 2.

Each sector S7-S12 (and also each sector S1-S6 not shown) comprises a number of memory cells 30 arranged in rows and columns. In known manner, all the cells 30 in each sector present the source terminal connected to the same common source line 20, and the cells 30 in the same row of cells present the control gate terminal connected to the same word line 31 (in common with all the cells in the same row of cells in the adjacent sectors). The cells 30 in the same column of cells present the drain terminal connected to one of the two local bit lines, and more specifically in such a manner that, in the direction of word lines 31, the cells connected to a local bit line 25 alternate with those connected to a local bit line 26.

Each pair of local bit lines 25, 26 is connected to the respective global bit line 13 by a selection transistor 32, 33 with its gate terminal connected to a control line 16. More specifically, the transistors 32 in each sector (interposed between the global bit lines 13 of the sector and a respective local bit line 25) are all connected to the same control line 16; and the transistors 33 in each sector (between global bit lines 13 and respective local bit lines 26) are all connected to a different control line 16 (as shown in more detail for sectors S7 and S10). As such, in the example shown, in which each sector row 11 comprises three sectors (or compound sectors, in the case of sectors S1-S6), six control lines 16 are sufficient for each sector row 11.

Control lines 16 preferably extend in the gap normally existing between two different sector rows 11, preferably in the form of first-level metal lines. In the example shown, common source lines 20 extend in the gap normally existing between two different sector columns 12, but in the alternative, in the event the global bias lines are the word lines, the gap between the columns may be occupied by control lines for the selection transistors of associated local word lines, which is the solution adopted, for example, when gate stress cannot be disregarded.

With the memory array structure shown in Figures 2 and 3, it is possible to read a sector in a given row and column 11, 12, and erase another in a different row and column. The possibilities afforded by the local decoding system shown are illustrated schematically in Figure 4 relative to a sector configuration as shown in Figures 2 and 3. More specifically, and as shown in Figure 4, performance of an operation (read, write, erase) in sector S1 or S2 (i.e. access to sector S1 or S2) permits simultaneous performance of an operation in (i.e. access to) one of sectors S8, S11, S9, S12; access to sector S3 or S4 permits simultaneous access to one of sectors S9,

S12, S7, S10; and access to sector S5 or S6 permits simultaneous access to one of sectors S8, S11, S7, S10.

For example, to erase data sector S3 without interrupting performance of the program memorized in program sectors S9 and S12, which must therefore remain accessible when erasing sector S3, it is possible to maintain common source line 20 connected to sector S3 at 12 V, and all the rows of sector S3 at 0 V, while finite state machine 7 (Figure 1) controls the erase duration. At the same time, finite state machine 7 provides for addressing the rows and columns of sectors S9 and S12 to read the program (or perform other operations).

According to a further aspect of the present invention, a row decoder is proposed, which is capable of addressing two different rows at the same time without fully duplicating the relative circuits, and as shown in Figure 5 described below.

The row decoder 3 in Figure 5 comprises a number of decoding sections 34 equal to the number of sector rows 11 (in this case, three, of which only two are shown); and each decoding section 34 comprises a multiplexer 35 presenting 2n data inputs, where n equals the number of bits required to address all the rows in the memory array. The data inputs of multiplexers 35 are connected to two groups of n address lines 36, 37, each coding a different address; and multiplexers 35 also comprise m selection inputs connected to m selection lines 38 for specifying which multiplexers 35 are to use which of the two addresses on lines 36 and 37, to simultaneously address two different rows in array 2. In other words, by means of selection lines 38, each multiplexer knows whether it is to output the address on line 36, the address on line 37, or no address at all.

Multiplexers 35 therefore present a first number of outputs 41 (equal to n/2), and a second number of outputs 42 (equal to n/2). Outputs 41 are connected directly or inversely to the inputs of a NAND gate 39, and code a first half of the address specified on lines 36 or 37; and outputs 42 are connected to a logic unit 40, and code a second half of the address specified on lines 36 or 37. Logic unit 40 is also connected to the output 43 of NAND gate 39. Logic unit 40 substantially comprises a combining circuit (in addition to a level shift circuit) with a number of outputs equal to the rows in the relative sector column 12; and forms a two-level decoding circuit together with NAND gate 39. In practice, NAND gate 39, with its direct or inverted inputs, decodes the first half-address, and logic unit 40 decodes the second half-address, also using the output of NAND gate 39.

Each output of each logic unit 40 is connected to a first input of a respective inverter 45, which presents a second input connected to a node 46, and an output connected to a word line 31. Row decoder 3 comprises three nodes 46 - one for each sector row 11; each node 46 is connected to two supply lines 50, 51 by respective P-channel MOS supply selection transistors 47, 48; and transistors 47, 48 present the control terminal connected to an enabling unit 49 (one for each sector row 11).

Line 50 supplies the voltage V_{CC} for reading the cells, while line 51 supplies the erase voltage V_{PP} or verify voltage V_V for erasing and/or writing the cells.

Each enabling unit 49 substantially comprises a pair of switches 52, 53 - one for each respective supply selection transistor 47, 48 - for connecting or disconnecting the control gate of respective transistors 47, 48 to ground, and so turning the transistors on or off. Switches 52, 53 are controlled by control signals supplied by control unit 7 over enabling lines 54 (in this case, six in number, equal to the number of transistors 47, 48 and switches 52, 53) for controlling the state of switches 52, 53 and hence transistors 48, 49 supplying inverters 45. Inverter 45, enabled by its logic unit 40 on the basis of the address specified on lines 36 or 37, therefore biases respective word line 31 at the voltage on line 50 or 51, as specified by the control signals on lines 54; and, by virtue of duplicating address lines 36, 37, and by virtue of lines 38 controlling multiplexers 35 as described above, it is possible to send two different addresses over lines 36 and 37, and to address two different lines 31 in different sector rows 11 to perform two instructions simultaneously.

As is known, memory array outputs are currently organized so that the bits in the same word are distributed along one row (belonging to different sectors). Conversely, according to a further aspect of the present invention, the outputs of memory array 2 are concentrated in the same sector. One embodiment of a column decoder implementing this type of organization is shown in Figure 6 wherein, on account of the different number of cells per row in sector S12 with respect to sectors S10 and S11, and hence the different number of global bit lines extending from these sectors, the bit lines extending from sector S12 (and similarly from sectors S9, S5, S6) are decoded at two levels.

In Figure 6, each sector is assumed to present sixteen outputs corresponding to sixteen bits to be sent to sense amplifiers 5; sectors S10 and S11 (and the corresponding sectors in the same sector column 12) are assumed to be connected to sixteen global bit lines; and sector S12 is assumed to be connected to forty-eight global bit lines. The architecture described below, however, may also be applied to different configurations with a different number of outputs (e.g. eight) and/or a different number of bit lines extending from the sectors.

The decoder 4 in Figure 6 therefore comprises sixteen output lines B1, B2, ..., B16 (corresponding to the sixteen bits in each word) connected at one end to sense amplifiers 5, and at the other end to the global bit lines 13 of the array sectors via selection transistors 58-60. More specifically, the sixteen global bit lines 13 from sectors S10 and S11 are each connected to a respective output line B1-B16 by a respective first selection transistor 58, so that the first global bit line 13 of sector S10 is connected to the first global bit line 13 of sector S11 and to the first output line B1, the second global bit

line 13 of sector S10 is connected to the second global bit line 13 of sector S11 and to the second output line B2, and so on. The selection transistors 58 on the global bit lines of sectors S10, S11 connected to the same output line B1-B16 are controlled by the same control signal YN1-YN16 supplied over a respective control line 62 connected to control unit 7.

Triplets 63 of global bit lines 13 of sector S12 are also connected to output lines B1-B16 by second selection transistors 60 controlled by respective signals YM1-YM16 supplied over control lines 64 also connected to control unit 7; and the three global bit lines 13 of sector S12 in the same triplet 63 (connected to the same output line B1-B16) are controlled by a respective third selection transistor 59. More specifically, the selection transistors 59 connected to the first global bit line in each triplet 63 are controlled by signal YN1 controlling the first global bit lines of sectors S10, S11; the selection transistors 59 connected to the second global bit line in each triplet 63 are controlled by signal YN2; and the selection transistors 59 connected to the third global bit line are controlled by signal YN3.

Consequently, to read the cells or some of the cells in a row in sector S10, row decoder 3 selects the row; local decoder 17 selects the columns (local bit lines 14 in Figure 2, lines 25 or 26 in Figure 3) in sector S10; and selection transistors 58 provide for selectively connecting the selected columns to the selected output line/s B1-B16 by means of signals YN1-YN16. Not being selected by local decoder 17, the other sectors S1-S9, S11 and S12 in no way interfere with the reading. Conversely, to read the cells or some of the cells in sector S12, selection transistors 60 only connect to output lines B1-B16 the triplet/s 63 of lines 13 specified by signals YM1-YM16; and, within each triplet 63, transistors 59 connect the global bit line 13 to be connected to the output. In this case also, sectors S1-S11 in no way interfere with the reading by not being selected by local column decoder 17.

Column decoder 4, however, only provides for successively reading two sectors, and must therefore be duplicated to permit two sectors in two different sector columns 12 to be read simultaneously. According to a further aspect of the present invention, therefore, a further column decoder and a further sense amplifier unit are provided. Since the architecture according to the invention is typically designed to permit reading of one sector and erasure or writing of another sector in a different sector column 12, the memory may be so controlled that one sense amplifier is only active during the erase verify procedure, and the other sense amplifier is only active during the read procedure. In which case, the sense amplifiers may be specialized according to the function to be performed, so as to eliminate, within each sense amplifier, the circuits relative to the discarded function, and employ the additional space for forming the additional decoding and sense units.

The architecture so formed is shown in Figure 7, which shows a read column decoder 65; a read sense amplifier unit 66; an erase column decoder 67; an erase sense amplifier unit 68; units 6 and 7 of the Figure 1 architecture; local column decoder 17 or 17' as in Figure 2 or 3; and source decoder 21 as in Figure 2. Read units 65 and 66 are arranged in the same way as corresponding units 3, 4 in the Figure 1 architecture; and erase units 67 and 68 are located on the opposite side of memory array 2, 2' in relation to units 65, 66. More specifically, erase column decoder 67 is connected to the top end of global bit lines 13 (arrow 70), and is controlled by control unit 7 in the same way as unit 4; and erase amplifier unit 68 is connected downstream from unit 67, and receives control signals from, and supplies output signals to, control unit 7.

Read and erase column decoders 65, 67 preferably present the same structure as unit 4, while sense amplifier units 66, 68 are specialized, as described above, so that each only includes the circuits relative to a respective function (read and verify).

To read, for example, sector S12 and verify sector S1 during erasure, the cell or cells in sector S12 to be read are appropriately biased by read column decoder 65, local column decoder 17', and row decoder 3; and, similarly, the cells in sector S1 to be verified are appropriately biased by erase column decoder 67, local column decoder 17', and row decoder 3 which therefore simultaneously addresses two different rows in the array - preferably as described with reference to Figure 5 - on the basis of two different addresses supplied over lines 36 and 37. Decoding (and reading) during writing are preferably performed by erase units 67, 68.

The architecture of the memory according to the present invention provides for increasing the number of sectors to meet different user requirements. Additional data sectors, in fact, may be provided using the same control circuitry and by simply increasing the size of the row decoder, as shown in Figure 8 which shows only a memory array 2 and row decoder 3. In addition to sectors S1-S12, array 2 also presents further sectors SA, SB, SC, SD, SE, SF presenting respective local bit lines 14 or 25, 26 (like sectors S1-S12) and connected to the same global bit lines 13 as sectors S1-S12 by respective selection switches 15 controlled by respective control lines 16.

If the row decoder is formed so as to independently address the rows of sectors SA-SF (for example, by adding a multiplexer 35 and relative circuits to the Figure 5 embodiment), it is possible, for example, to read sector SA and simultaneously erase sector S4.

The proposed architecture provides for so addressing the memory space as to mask the noncontiguous arrangement of the sectors and so give the customer the impression of working with a contiguous sector arrangement.

For this purpose, a map table need simply be provided upstream from control unit 7, to relate the actual noncontiguous arrangement of the sectors to the apparent contiguous one. This is shown schematically in Figure 9, which shows only control unit 7 and map table 73

of memory 1. Map table 73 receives the addresses supplied externally and relative to the "ideal" arrangement required by the customer (arrow 7a), and supplies the actual internal addresses corresponding to the real arrangement of the sectors (arrow 75). The actual addresses 75 may also be supplied directly to the row and column decoders.

Map table 73 may be formed in any way, as a logic circuit or a memory element; and, in the latter case, it may be implemented by a special memory array, or using a portion of memory array 2 as shown schematically in Figure 9.

Consequently, as opposed to a linear sector arrangement, as in the known memory map in Figure 9a, an arrangement is achieved which is better suited to the requirements of the user, as shown in Figure 9b, and which provides for more conveniently organizing the memory space, for example, by maintaining the program storage sectors adjacent to the data sectors.

Moreover, in the case of a map table 73 in the form of an erasable, reprogrammable memory, it may be programmed freely by the customer, who may alter the relative position of the sectors within the memory space as required.

The proposed architecture provides for troublefree column redundancy control, and the addition of further sectors, with no additional circuitry, for enabling or reading redundancy column addresses. One solution is shown in Figure 10 in which, in addition to program and data sectors S1-S12, memory array 2 also comprises sectors SA-SF similar to those in Figure 8; and sectors S1-S12 and SA-SF comprise redundancy columns connected to respective global bit lines. Memory 1 also comprises a fail column memory 80; and a redundancy control unit 81 which is supplied by control unit 7 (arrow 83) with the addresses of the (read or write) enabled cells, and by fail column memory 80 (arrow 82) with the addresses of the fail columns. Redundancy control unit 81 then compares the incoming addresses, and, in the event they match (fail column addressed), disables, over line 84, the read and erase column decoders 65, 67, and enables, over line 85, a special redundancy decoder 86 output connected to read and erase sense amplifiers 66, 68. This operation provides for disabling the fail column via decoders 65, 67, and for enabling and substituting the corresponding redundancy column via redundancy decoder 86, thus maintaining the structure of memory 1, regardless of whether it is expanded by sectors SA-SF or presents the basic structure composed, for example, of sectors S1-S12.

Alternatively, instead of making the whole column redundant in the event of failure of only a portion of it (local bit line), it is possible to make only the failed local bit line, e.g. of sector S7, redundant, and not those of the sectors SB, S2 and S10 connected to the same global bit line. In this case, however, the greater adaptability of the memory to cope with a larger number of fail conditions demands a more complex control logic.

According to a further variation, redundancy decoder 86 may be dispensed with, and the redundancy control unit made to control column decoders 65, 67 to address the redundancy global bit lines as opposed to the failed addressed ones.

As compared with known solutions comprising redundancy sectors, the architecture according to the invention presents the advantage of making only the fail columns in a specific sector redundant, instead of a whole column of cells belonging to superimposed sectors, thus reducing the number of rows required in the redundancy sectors and hence the size of the memory as a whole.

The advantages of the memory device according to the invention will be clear from the foregoing description. In particular, the architecture described provides for operating simultaneously in two sectors of the memory array, thus greatly reducing memory access time, especially when erasing a sector; presents a high degree of modularity; and permits remapping of the sectors and hence troublefree use and straightforward redundancy operations.

Clearly, changes may be made to the memory device as described and illustrated herein without, however, departing from the scope of the present invention. In particular, the solutions described may be applied to an isolated, preferably flash, memory device, as well as to memories integrated in microcontrollers and dedicated memories such as ASM (Application Specific Memory) devices; and the global bias lines connected to local bias lines may also be word lines instead of or in addition to bit lines.

Claims

1. A memory device (1) comprising a memory array (2) including a number of memory cells (30) grouped into a plurality of sectors (S1-S12); characterized in that it comprises means (14, 15, 17) for simultaneously addressing at least two said sectors of said memory array.

2. A device as claimed in Claim 1, wherein said sectors (S1-S12) are arranged in rows of sectors (11) and columns of sectors (12), and form first lines of sectors extending in a first direction, and second lines of sectors extending in a second direction perpendicular to the first direction; characterized in that it comprises global bias lines (13) extending parallel to said first direction and substantially along the whole length of said first lines of sectors; a plurality of local bias lines (14; 25, 26) for each said global bias line, said local bias lines extending parallel to said first direction and being at least equal in number to the sectors forming said first lines of sectors; a plurality of sector selection means (15; 32, 33) interposed between each local bias line and a respective global bias line; and control means (17,

17') for said selection means for separately controlling said sectors.

3. A device as claimed in Claim 2, characterized in that said sector selection means comprise sector selection transistors (15; 32, 33) having a control terminal connected to control lines (16) in turn connected to local decoding units (17, 17'); at least one said control line being provided for each sector (S1-S12).

4. A device as claimed in Claim 3, characterized in that said global bias lines are global bit lines (13); said local bias lines are local bit lines (14; 25, 26); and said local decoding units are column decoding units (17, 17') controlled by a control unit (7) of the memory device (1).

5. A device as claimed in Claim 4, characterized in that said control lines (16) extend between adjacent rows of sectors (11).

6. A device as claimed in Claim 4 or 5, characterized in that it comprises a first (25) and second (26) local bit line for each global bit line (13) and for each sector (S1-S12); and said sector selection transistors comprise first sector selection transistors (32) located between each global bit line and the respective first local bit line, and second sector selection transistors (33) located between each global bit line and the respective second local bit line; said first sector selection transistors in the same sector being connected to the same first control line (16); and said second sector selection transistors in the same sector being connected to the same second control line (16).

7. A device as claimed in one of the foregoing Claims from 4 to 6, and comprising a row decoding unit (3) formed of a plurality of decoding sections (34); characterized in that each said decoding section comprises two pluralities of address inputs, and one plurality of address selection inputs; each said plurality of address inputs being connected to a respective plurality of address lines (36, 37) to supply each said decoding section with two different row addresses; and said address selection inputs being connected to respective address selection lines (38), to supply each section (34) of said decoding unit with information signals relative to which of the two addresses is to be used.

8. A device as claimed in one of the foregoing Claims from 4 to 7, wherein a digital word is formed of a plurality of bits, each memorized in a respective memory cell (35); characterized in that the memory cells relative to the same digital word all belong to the same sector (S1-S12).

9. A device as claimed in Claim 8, and comprising a column decoding unit (4; 65, 67) connected to said global bit lines (13); characterized in that said column decoding unit comprises a plurality of output lines (B1-B16); each output line being connected to a plurality of global bit lines belonging to different columns of sectors (12).

10. A device as claimed in Claim 9, characterized in that said column decoding unit (4; 65, 67) comprises a plurality of first bit selection transistors (58) along said global bit lines (13); all said first bit selection transistors relative to global bit lines (13) connected to a same output line (B1-B16) being controlled by a same selection signal (YN1-YN16).

11. A device as claimed in Claim 9 or 10, characterized in that at least one column of sectors (12) comprises a number of global bit lines (13) greater than the number of said output lines (B1-B16); and said global bit lines in said at least one column of sectors are grouped into groups of lines (63); the global bit lines in one group of lines being connected together, and being connected to the respective output line by a second bit selection transistor (60).

12. A device as claimed in Claim 10, characterized in that it comprises third bit selection transistors (59) located along said global bit lines (13) in groups of lines (63), and controlled by said selection signal (YN1-YN16) controlling said first selection transistors.

13. A device as claimed in any one of the foregoing Claims from 4 to 12, characterized in that it comprises a first and second column decoding unit (65, 67) connected to said global bit lines (13); and a first and second sense amplifying unit (66, 68) respectively connected to said first and second column decoding unit.

14. A device as claimed in Claim 13, characterized in that said first column decoding and sense amplifying units (65, 66) are activated during a reading step; and said second column decoding and sense amplifying units (67, 68) are activated during an erasing and writing step.

15. A device as claimed in any one of the foregoing Claims from 4 to 14, characterized in that it comprises a mapping unit (73) presenting a plurality of address inputs supplied with customer sector address signals (7a), and a plurality of address outputs supplying real sector address signals (75); said mapping unit memorizing the correlation between said customer sector address signals and said real sector address signals.

16. A device as claimed in Claim 15, characterized in that said mapping unit (73) comprises a nonvolatile memory.

17. A device as claimed in Claim 16, characterized in that said nonvolatile memory (73) is formed by a portion of said memory array (2).

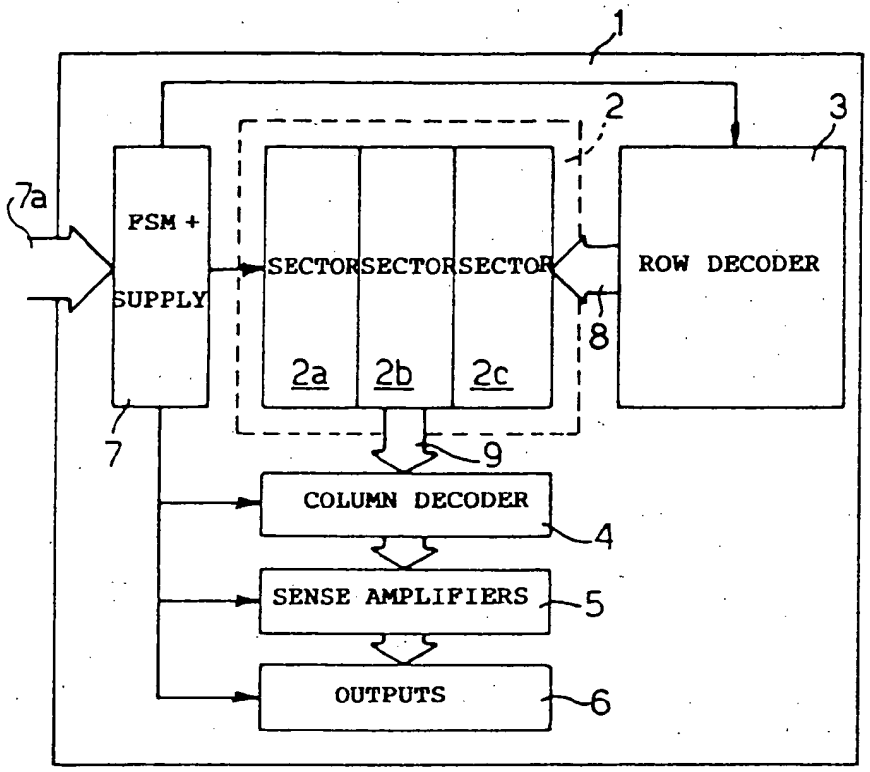
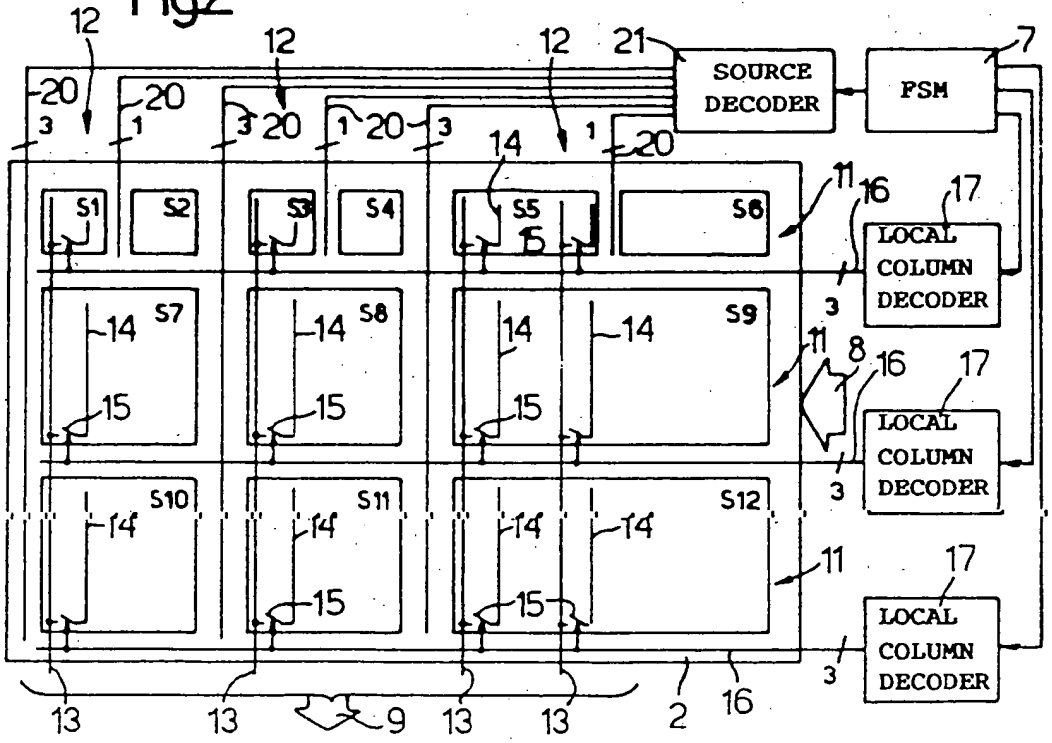


Fig.1

Fig2



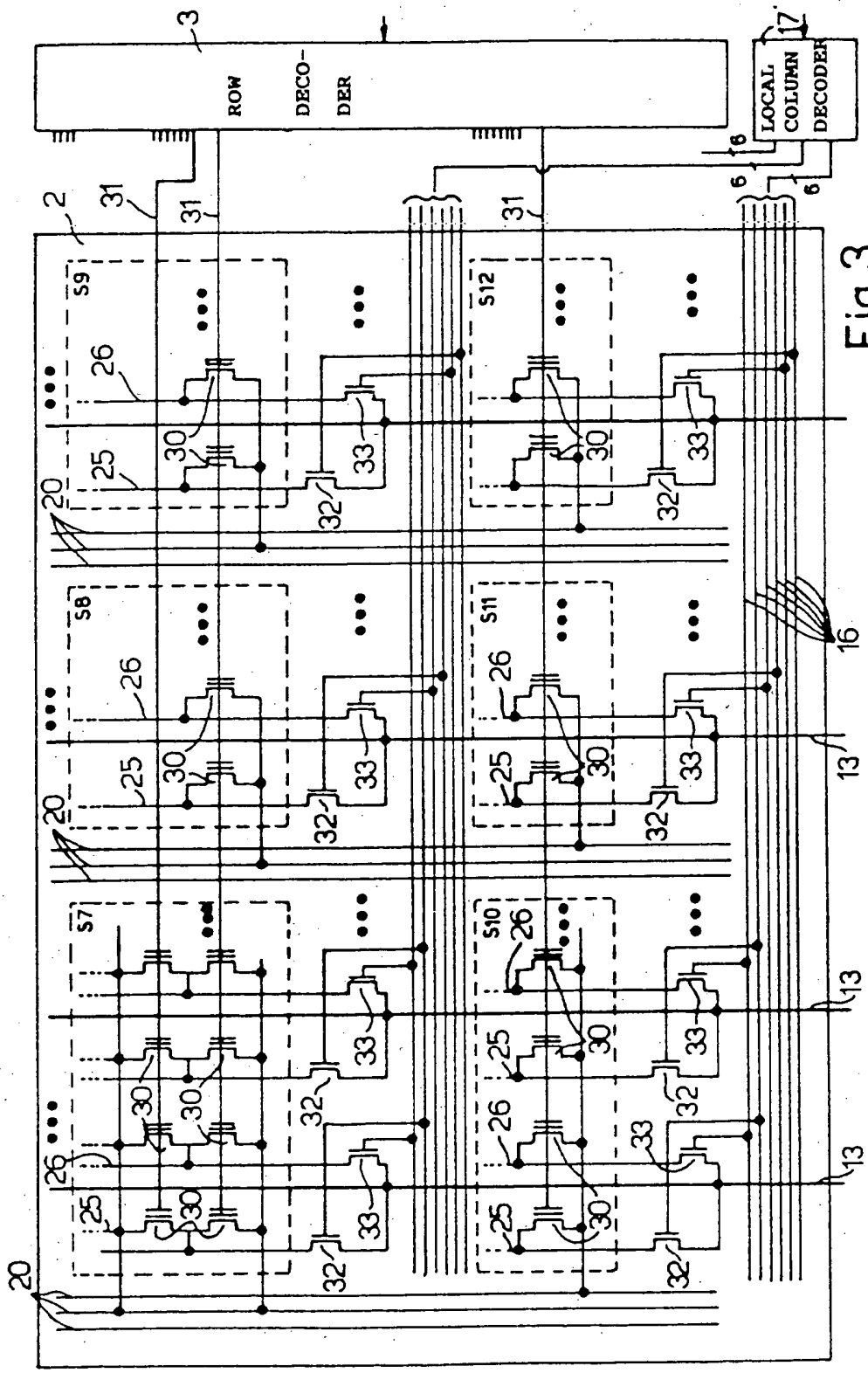


Fig.3

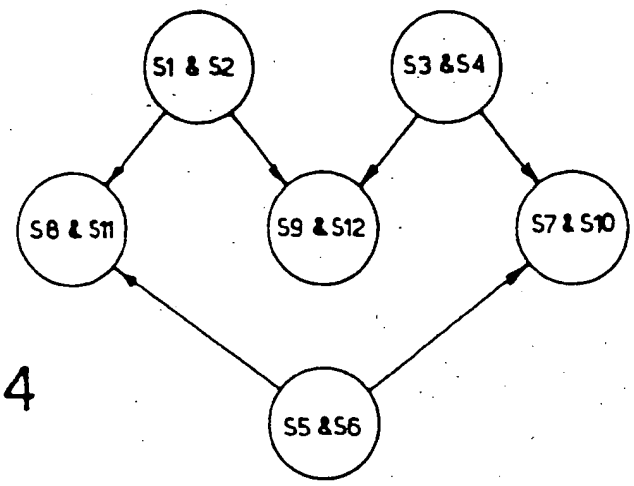
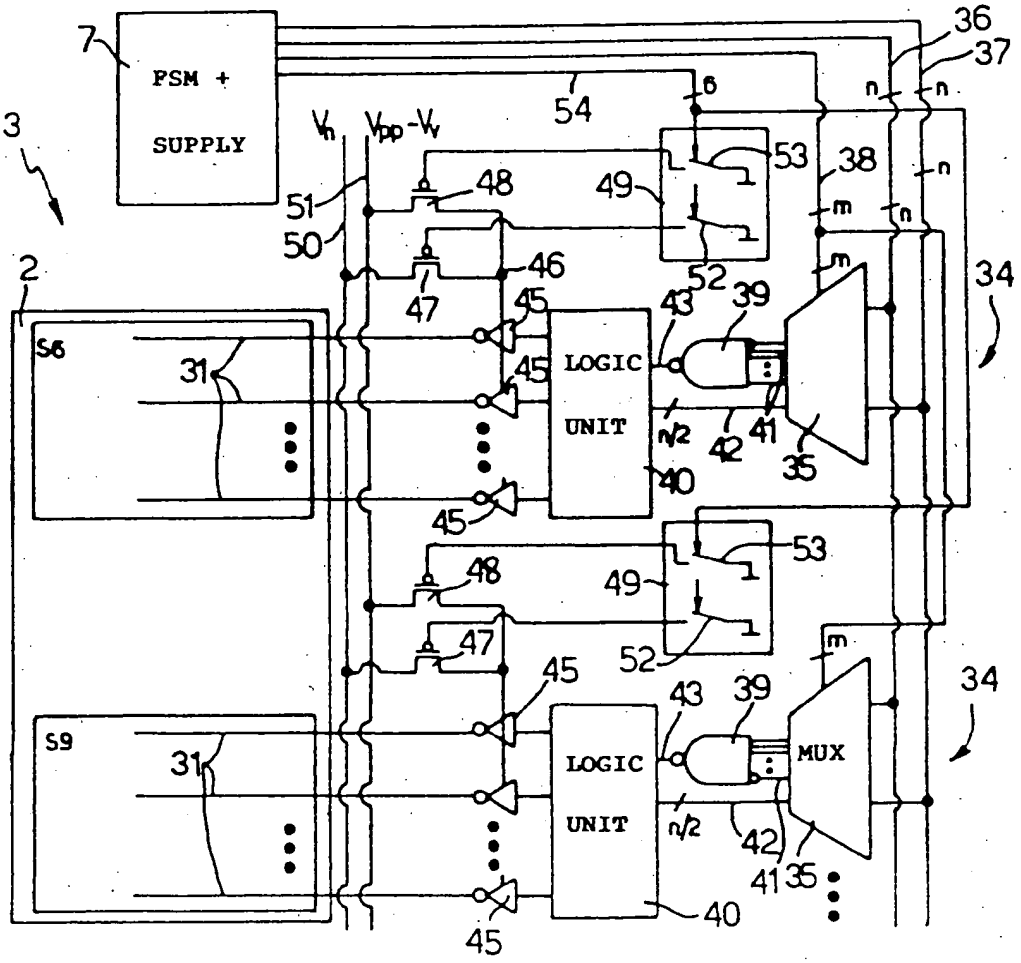


Fig.4

Fig.5



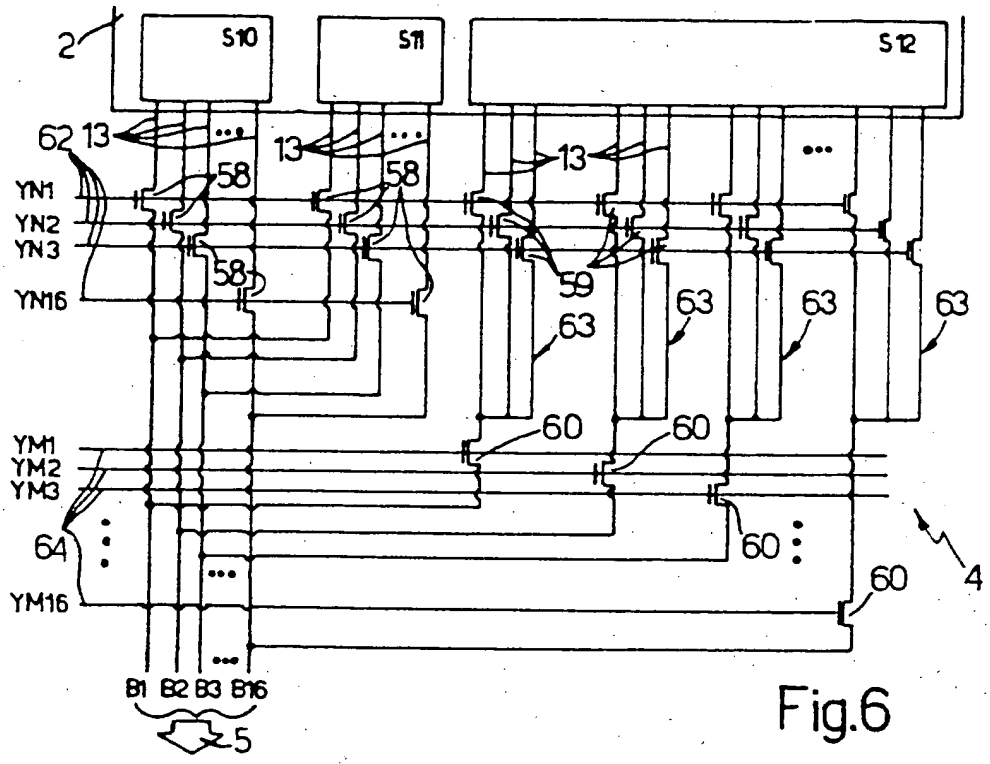
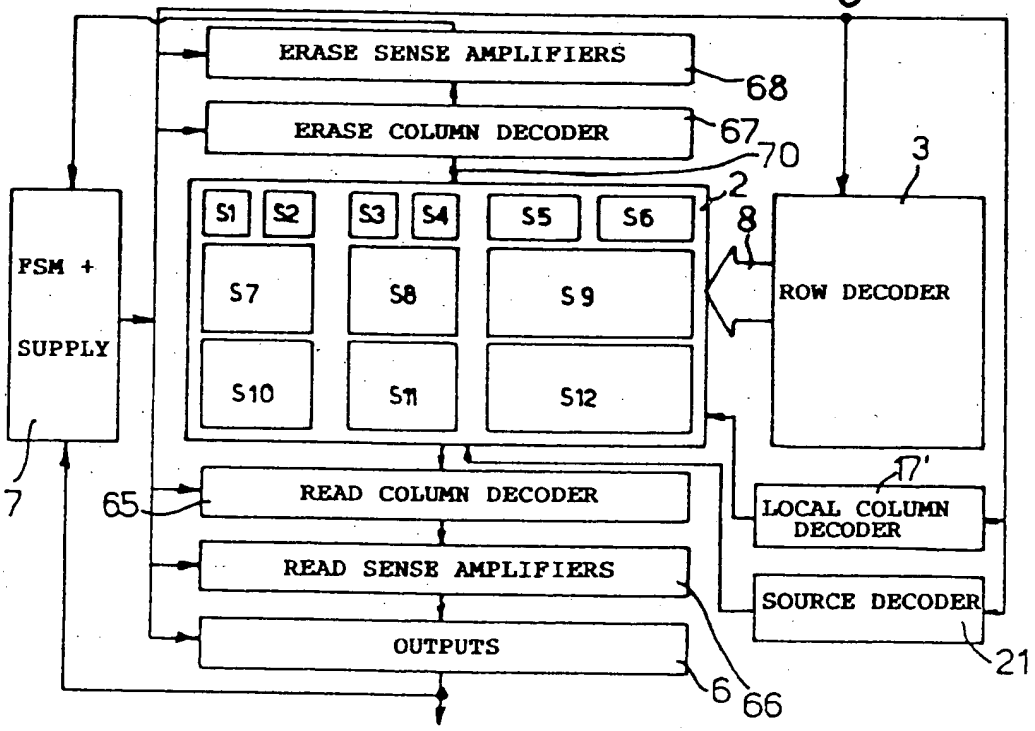


Fig.6

Fig.7



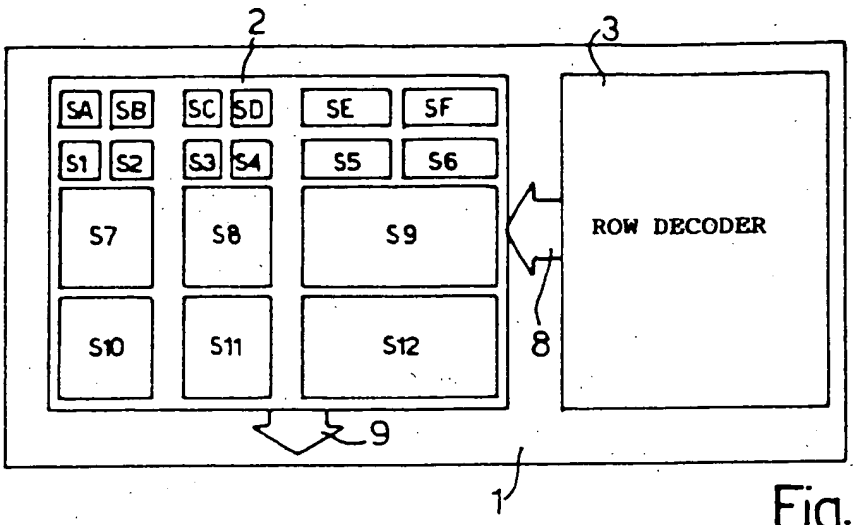


Fig. 8

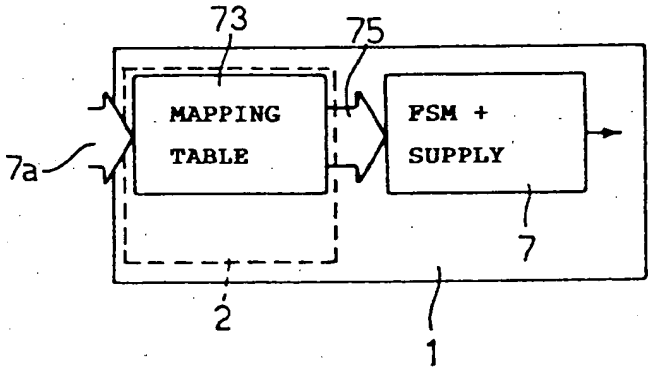


Fig. 9

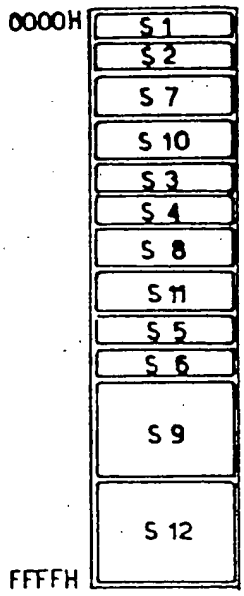


Fig. 9a

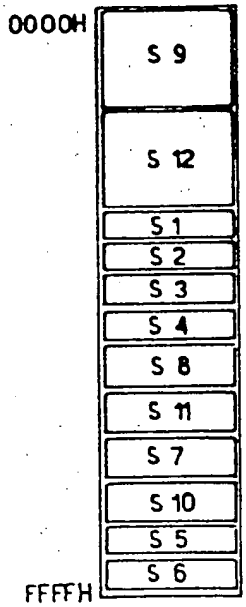


Fig. 9b

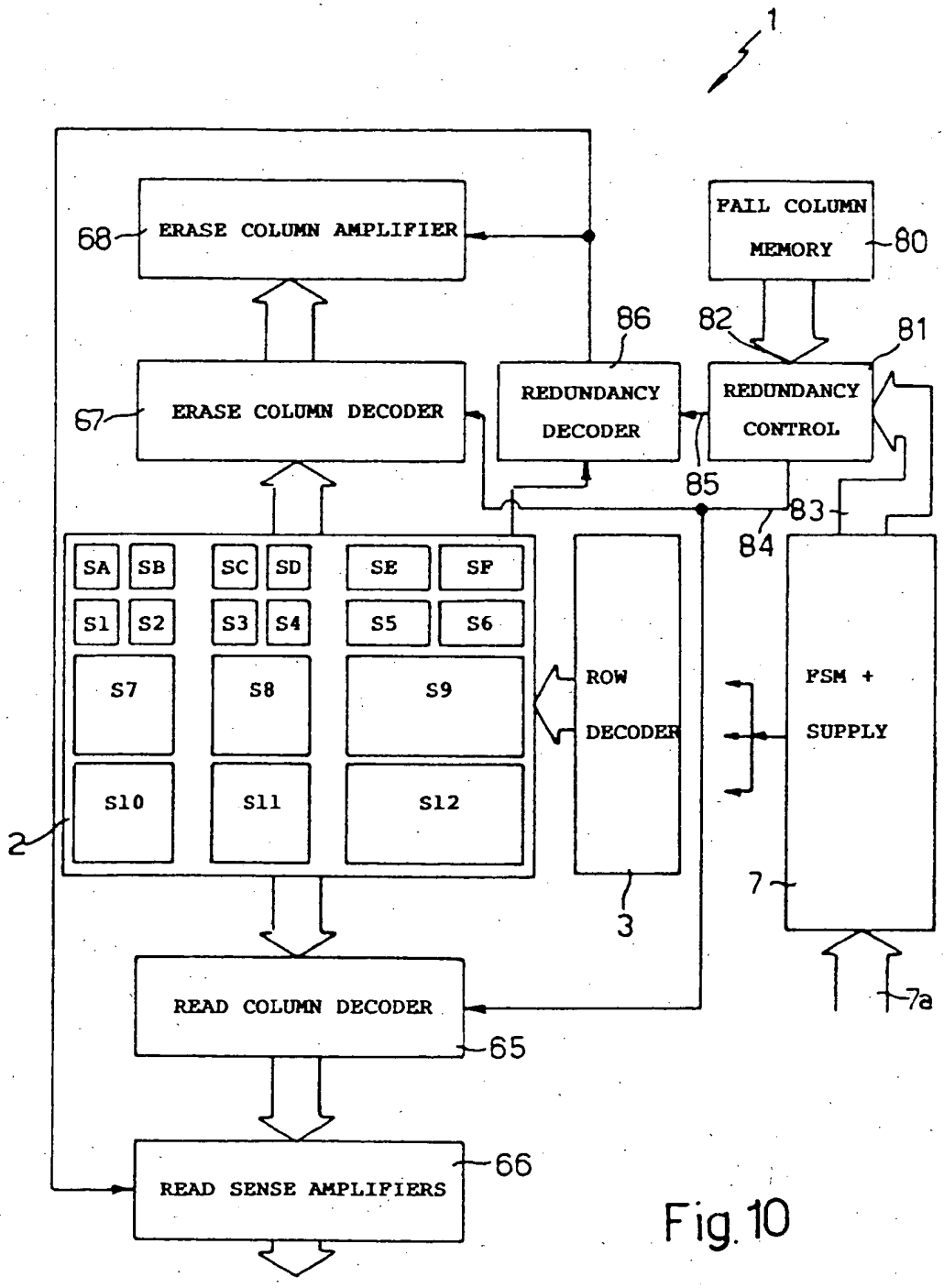


Fig. 10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0183

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	US-A-5 245 572 (KOSONOCKY ET AL) * column 3, line 19 - column 13, line 35; figures 2,3 *	1 2-5	G11C8/00 G11C7/00 G11C16/06
X A	EP-A-0 540 363 (INTERNATIONAL BUSINESS MACHINES CORPORATION) * column 2, line 34 - column 3, line 14; figures 1,2 * * column 5, line 2 - line 55; figures 11-14 *	1 2,8	
X	PATENT ABSTRACTS OF JAPAN vol. 16, no. 231 (P-1361) 28 May 1992 & JP-A-04 049 595 (HITACHI LTD.) 18 February 1992 * abstract *	1	
Y	WO-A-94 17528 (YU) * page 7, line 34 - page 22, line 6; figures 3-9 *	2-5	
A	EP-A-0 618 586 (SONY CORPORATION) * column 6, line 38 - column 8, line 2; figures 3,5 *	2-6	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G11C

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 October 1995	CUMMINGS A.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid,

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions,

namely:

See Sheet B.

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.

namely claims:

☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

namely claims: 1-6, 8

European Patent Office

EP95830183.0 Sheet B.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

Claims 1-6,8 :Memory organised in sectors with local and global bit lines.

Claims 7,9-14:Structures of row and column decoders

Claims 15-17 :Mapping of logical sector addresses to physical sectors.